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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/733,095	12/11/2003	Wang-Jin Chen	250606-1020	9153

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EXAMINER	
ROSSOSHEK, YELENA	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 05/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/733,095	CHEN ET AL.	
	Examiner	Art Unit	
	Helen Rossoshek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,6,7,9,11,13 and 15* is/are rejected.

7)☒ Claim(s) *3,5,8,10,12,14 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Application 10/733,095 filed 12/11/2003 and amendment filed 03/05/2006.

2. Claims 1-16 remain pending in the Application.

3. Applicant's arguments have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Iwasa (US Patent 6,721,933).

Claim Objections

4. Claim 13 is objected to because of the following informalities: fourth limitation is formulated unclear to what Applicant intend to mean in term of "between the loop of I/O circuits" and what? For the examination purposes Examiner considers this limitation according to the Figure 2 of the instant Application, such as row (22) of I/O circuits disposed between the loop (21) of I/O circuits and row 23 of I/O circuits.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1, 2, 4, 6, 7, 9, 11, 13, 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Iwasa (US Patent 6,721,933).

With respect to claims 1, 6 Iwasa teaches an I/O circuit placement method for placing I/O circuits included in a semiconductor device within a semiconductor device and an input/output cell placement method for arrangement I/O cells on a chip (abstract; col. 1, ll.12-14), comprising a step of: placing at least two rows of I/O circuits on a first side of a chip within three rows of the I/O cells 120_1-120_6, 120_2-120_5, 120_3-120_4 arranged on a semiconductor chip 110 as shown on the Fig. 2 (col. ll.22-25), wherein each I/O circuit has a head section and a tail section within I/O cells 120_1-120_5 containing driver circuit sections 130_1-130_3 (tail) and interface sections 132_1-132_3 (head) (col. 7, ll.59-61), the head section and the tail section are arranged in a column direction perpendicular to a row direction of the I/O circuits as shown on the Fig. 2 , wherein driver circuit sections 130_1-130_3 (tail) and interface sections 132_1-132_3 (head) placed that their direction is perpendicular to the direction the I/O cells placed (col. 8, ll.27-32), the tail section transfers signals to and from external devices within driver circuit sections 130_1-130_3, wherein driver circuits for transferring a signals from outer peripheral portion of the chip toward the chip core (col. 7, ll.62-67, col. 8, ll.1-4; col.4, ll.26-30) and the head section severs an interface circuit between the tail section and a core circuit region to convert signal level within interface sections 132_1-132_3 including level shifter circuits for converting signals between driver circuit section (tail) and basic cells formed in the core region (col. 8, ll.6-10).

With respect to claim 13 Iwasa teaches a semiconductor device (abstract), comprising: a chip within semiconductor chip 110 shown on the Figs. 1-3 (col. 6, ll.62-64); a core circuit region disposed on the chip within core region 112 as shown on the Fig. 1 (col. 6, ll.62-64); a loop of I/O circuits disposed at the periphery of the chip and around the core circuit region as shown on the Fig. 2, wherein loop of plurality of I/O cells placed in the placement region 114 between plurality of pads 122 and core region 112; and at least one row of I/O circuits disposed between the loop of I/O circuits within middle row of I/O cells 120_2, in the loop of the I/O cells as shown on the Fig. 2, wherein each I/O circuit has a head section and a tail section within driver circuit sections 130_1-130_3 (tail) and interface sections 132_1-132_3 (head) as shown on the Fig. 2 (col. 7, ll.59-61), the placement direction of the head section and the tail section is perpendicular to that of the I/O circuits in the loop or the row within driver circuit sections 130_1-130_3 (tail) and interface sections 132_1-132_3 (head) placed that their direction is perpendicular to the direction the I/O cells placed (col. 8, ll.27-32).

With respect to claims 2,4, 7, 9, 11, 15 Iwasa teaches:

Claims 2, 7: further comprises a step of placing another row of I/O circuits on a second side of the chip as shown on the Fig. 2, wherein loop of plurality of I/O cells placed in the placement region 114 between plurality of pads 122 and core region 112, wherein loop is arranged on each side of the chip;

Claims 4, 9, 15: wherein the head sections are oriented to the head sections in the adjacent tows as shown on the Fig. 2 wherein head 132_1 of the I/O cell 120_1 oriented to the head 132_6 of the I/O cell 120_6;

Claim 11: wherein the core circuit region is disposed on the chip as shown on the Fig. 1, and the rows of I/O circuits are disposed outside the core circuit region and are at the periphery of the chip as shown on the Fig. 1 (col. 4, ll.26-30).

Allowable Subject Matter

7. Claims 3, 5, 8, 10, 12, 14, 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record does not teach placement of the I/O cells that the head sections are oriented to the tail sections in the adjacent row (claims 3, 8, 14), or the tail sections are oriented to the tail sections in the adjacent tows (claims 10, 16); a different number of I/O cells are placed on different row as claimed (claims 5, 12).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner
Helen Rossoshek
AU 2825

SUN JAMES LIN
PRIMARY EXAMINER